

9/28/05

US 5,283,761

09/654367

WELCOME to QUESTEL.ORBIT- Your Guide to INTELLECTUAL PROPERTY

Query/Command : file pluspat

Selected file: PLUSPAT

Search statement 1

Query/Command : us5283761/pn

\* SS 3: Results 1

Search statement 4

Query/Command : prt fu legalall max

1 / 1 PLUSPAT - @QUESTEL-ORBIT - image  
PN - US5283761 A 19940201 [US5283761]  
TI - (A) Method of multi-level storage in DRAM  
PA - (A) MOSAID TECHNOLOGIES INC (CA)  
PAO - Mosaid Technologies Incorporated, Ontario [CA]  
IN - (A) GILLINGHAM PETER B (CA)  
AP - US91667392 19920722 [1992US-0916673]  
PR - US91667392 19920722 [1992US-0916673]  
IC - (A) G11C-007/00  
EC - G11C-011/56E  
PCL - ORIGINAL (O) : 365189070; CROSS-REFERENCE (X) : 327051000  
365149000 365168000 365189090 365233500  
DT - Basic  
CT - US4287570; US4415992; US4661929; US4771404; US5184324  
STG - (A) United States patent  
AB - A method of processing data having one of four voltage levels stored in a DRAM cell is comprised of sensing whether or not the data voltage is above or below a voltage level midway between a highest and a lowest of the four levels, setting the voltage on a reference line higher than the lowest and lower than the next highest of the four levels in the event the data voltage is below the midway voltage level, and setting the voltage on the reference line higher than the second highest and lower than the highest of the four levels in the event the data voltage is above the midway point, and sensing whether the data voltage is higher or lower than the reference line, whereby which of the four levels the data occupies is read.

1 / 1 LGST - @EPO  
PN - US5283761 A 19940201 [US5283761]  
AP - US91667392 19920722 [1992US-0916673]  
ACT - 19920722 US/AS02-A  
ASSIGNMENT OF ASSIGNOR'S INTEREST  
OWNER: MOSAID TECHNOLOGIES INCORPORATED P.O. BOX 13579 KA;  
EFFECTIVE DATE: 19920707  
  
19920722 US/AS02-A  
ASSIGNMENT OF ASSIGNOR'S INTEREST  
OWNER: GILLINGHAM, PETER B.; EFFECTIVE DATE: 19920707

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19960514 US/RF-A  
REISSUE APPLICATION FILED  
EFFECTIVE DATE: 19960131  
UP - 2003-22

1 / 1 CRXX - @CLAIMS/RRX  
AN - 2441799  
PN - 5,283,761 A. 19940201 [US5283761]  
PA - Mosaid Technologies Inc CA  
PT - E (Electrical)  
ACT - 19960131 REISSUE REQUESTED  
ISSUE DATE OF O.G.: 19960514  
REISSUE REQUEST NUMBER: 08/595020  
EXAMINATION GROUP RESPONSIBLE FOR REISSUEPROCESS: 2511  
Reissue Patent Number: USRE37072

UP - 1999-00

Search statement 4

Query/Command : fam us5283761/pn

1 Patent Groups  
\*\* SS 4: Results 2

Search statement 5

Query/Command : famstate nonstop

1 / 2 PLUSPAT - @QUESTEL-ORBIT - image  
PN - USRE37072 E1 20010227 [USRE37072]  
STG - (E1) Reissue Patent  
TI - (E1) Method of multi-level storage in DRAM and apparatus thereof  
PA - (E1) MOSAID TECHNOLOGIES INC (US)  
PAO - Mosaid Technologies, Inc., Kanata [CA]  
IN - (E1) GILLINGHAM PETER B (CA)  
IC - (E1) G11C-007/00  
AP - US59502096 19960131 [1996US-0595020]  
PR - US59502096 19960131 [1996US-0595020]  
US91667392 19920722 [1992US-0916673]  
EC - G11C-011/56E  
PCL - ORIGINAL (O) : 365189070; CROSS-REFERENCE (X) : 327052000  
327056000 365149000 365168000 365189090 365190000  
DT - Corresponding document  
UP - 2001-14

2 / 2 PLUSPAT - @QUESTEL-ORBIT - image

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PR - US91667392 19920722 [1992US-0916673]  
EC - G11C-011/56E  
PCL - ORIGINAL (O) : 365189070; CROSS-REFERENCE (X) : 327051000  
365149000 365168000 365189090 365233500  
DT - Basic

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PN - US5283761 A 19940201 [US5283761]

AP - US91667392 19920722 [1992US-0916673]

ACTE- 19920722 US/AS02-A

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ASSIGNMENT OF ASSIGNOR'S INTEREST

OWNER: GILLINGHAM, PETER B.; EFFECTIVE DATE: 19920707

19960514 US/RF-A

REISSUE APPLICATION FILED

EFFECTIVE DATE: 19960131

UP - 2003-22

9/28/05

US RE 37,072

09/654367

WELCOME to QUESTEL.ORBIT- Your Guide to INTELLECTUAL PROPERTY

Query/Command : file pluspat

Selected file: PLUSPAT

Search statement 1

Query/Command : re37072/pn

\*\* SS 1: Results 1

Search statement 2

Query/Command : prt fu legalall max

1 / 1 PLUSPAT - @QUESTEL-ORBIT - image  
PN - USRE37072 E1 20010227 [USRE37072]  
TI - (E1) Method of multi-level storage in DRAM and apparatus thereof  
PA - (E1) MOSAID TECHNOLOGIES INC (US)  
PAO - Mosaid Technologies, Inc., Kanata [CA]  
IN - (E1) GILLINGHAM PETER B (CA)  
AP - US59502096 19960131 [1996US-0595020]  
FD - Reissued: US916673 19920722 [1992US-0916673]  
Reissue of: US5283761 - 19940201  
PR - US59502096 19960131 [1996US-0595020]  
US91667392 19920722 [1992US-0916673]  
IC - (E1) G11C-007/00  
EC - G11C-011/56E  
PCL - ORIGINAL (O) : 365189070; CROSS-REFERENCE (X) : 327052000  
327056000 365149000 365168000 365189090 365190000  
DT - Corresponding document  
CT - US4287570; US4415992; US4622655; US4661929; US4771404; US5184324;  
US5293563  
Ohta, Yoshiji et al., Symposium, "A Novel Memory Cell Architecture  
for High-Density DRAMs," VLSI Circuits, May 1989, pp. 101-102.  
STG - (E1) Reissue Patent  
AB - A method of processing data having one of four voltage levels  
stored in a DRAM cell is comprised of sensing whether or not the  
data voltage is above or below a voltage level midway between a  
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the midway voltage level, and setting the voltage on the reference  
line higher than the second highest and lower than the highest of  
the four levels in the event the data voltage is above the midway  
point, and sensing whether the data voltage is higher or lower  
than the reference line, whereby which of the four levels the data  
occupies is read.  
UP - 2001-14

1 / 1 CRXX - @CLAIMS/RRX  
AN - 3466983  
PN - 37,072 E 20010227 [USRE37072]  
PA - Mosaid Technologies Inc CA  
PT - E (Electrical)

9/28/05

US RE 37,072

09/654367

ACT - 20011218 CERTIFICATE OF CORRECTION

UP - 2001-51

UCOR- 2001-12-18

Search statement 2

Query/Command : fam re37072/pn

1 Patent Groups  
\*\* SS 2: Results 2

Search statement 3

Query/Command : famstate nonstop

1 / 2 PLUSPAT - @QUESTEL-ORBIT - image  
PN - USRE37072 E1 20010227 [USRE37072]  
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DT - Corresponding document  
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DT - Basic

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19960514 US/RF-A  
REISSUE APPLICATION FILED  
EFFECTIVE DATE: 19960131  
**UP** - 2003-22